

REMARKS

The Non-Final Office Action of November 1, 2005 has been received and its contents carefully analyzed. By this amendment, claim 1 has been amended and claims 14 and 15 have been cancelled. Accordingly, claims 1-13 are currently pending in the application, of which claims 1 and 10 are independent claims. Applicants appreciate the indication that claims 5 and 7 contain allowable subject matter.

Applicants respectfully submit that the above amendments do not add new matter to the application and are fully supported by the specification. Support for the amendment(s) may be found at least in Figure(s) 9-12 and at page 6, line 23 to page 7, line 4; at page 7, lines 11-19; and at page 8, lines 7-15 of the specification.

Entry of the Amendment is proper under 37 C.F.R. §1.116 because it (a) places the application in *prima facie* condition for allowance for the reasons discussed herein; (b) does not raise new issues requiring further search and/or consideration by the Examiner because similar subject matter was previously considered by the Examiner and thus further consideration and/or search by the Examiner is not warranted; (c) places the application in better form for appeal, should an appeal be necessary; and (d) responds to formal matters set forth by the Examiner. For at least these reasons, entry of the present Amendment and Remarks is therefore respectfully requested. Accordingly, Applicants request reconsideration and timely withdrawal of the pending rejections for the reasons discussed below.

Rejections Under 35 U.S.C. § 102

Claims 10-15 stand rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by U. S. Patent No. 6,303,963 issued to Ohtani, *et al.* ("Ohtani"). Applicants respectfully traverse this rejection for at least the following reasons.

In order for a rejection under 35 U.S.C. §102 to be proper, a single reference must disclose each and every claimed feature. To be patentable, a claim need only recite a single novel features that is not disclosed in the cited reference. Thus, the failure of a cited reference to disclose one or more claimed features renders the 35 U.S.C. §102 rejection improper.

Claims 10-13

Claim 10 presently recites, "A flat panel display having a matrix-type array of sub-pixels, each of which comprises a thin film transistor...wherein the driving thin film transistor comprises semiconductor channels which are derived from a semiconductor layer, and heterogeneous straight lines are separated from each other on the semiconductor layer, and wherein each of the semiconductor channels comprises at least one of the heterogeneous straight lines."

In a non-limiting example and for purposes of discussion, heterogeneous straight lines, which have electrical properties, e.g. conductivity, that are different than other areas of the semiconductor, may be formed when a region of the semiconductor is subject to laser beam irradiation (See Application specification, page 2, lines 5-20).

Ohtani fails to teach each and every claim feature of independent claim 10, more particularly, Ohtani fails to teach each of the semiconductor channels comprising at least one of the heterogeneous straight lines. Rather, Ohtani teaches forming a semiconductor by crystallizing the semiconductor film using a catalytic element and then removing the catalytic element, thereby resulting in extremely small fluctuations in electrical characteristics such as threshold voltage (See col. 2, line 12 to col. 3, line 20). Thus, although Ohtani teaches formation of a semiconductor circuit, such teachings do not include or relate to the formation of heterogeneous straight lines, and more particularly to the formation of semiconductor channels comprising at least one of the heterogeneous straight lines, as recited in independent claim 10.

The Examiner alleges that heterogeneous straight lines are shown in FIGS. 2D, 6B-6E, and 7A-7D of Ohtani, further arguing that conventionally, when forming channels from an amorphous semiconductor layer, after laser crystallization, the amorphous semiconductor layer becomes a polycrystalline semiconductor with regions of crystallized and regions of less crystallized. The heterogeneous straight lines are defined at the boundary of the regions of the crystallized and regions of less crystallized (See Office Action, on page 6 and Figures from Attachment provided by Examiner).

Applicants respectfully disagree that FIGS. 2D, 6B-6E, and 7A-7D illustrate the existence of heterogeneous straight lines. Figures can only anticipate claims if they clearly show the structure which is claimed (See MPEP §2125). The figure must show all the claimed structural features and how they are put together (See MPEP §2121.04). The figures cited by the Examiner clearly do not illustrate the heterogeneous straight lines and the semiconductor channels comprising at least one of the heterogeneous straight lines.

With regard to the Examiner's response to Applicants' arguments (See Office Action, on page 6, and Figures from Attachment provided by Examiner), Applicants respectfully disagree with the Examiner's presentation that heterogeneous straight lines would be inherent from the conventional formation of channels from the amorphous semiconductor layer, wherein each of the semiconductor channels comprise at least one of the heterogeneous straight lines, as cited in independent claim 10. Rather, as taught by the Examiner, "the heterogeneous straight lines are defined at the boundary of the regions of the crystallized and regions of less crystallized" (See Office Action, on page 6, and particularly Figure 2 from Attachment provided by Examiner). "To establish inherency, the extrinsic evidence, 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill in the art.' *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d, 1949, 1950-51 (Fed. Cir. 1999) (citations omitted). "In relying upon the theory of

inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.” *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). Applicants respectfully submit that the Examiner has failed to meet such a burden of illustrating the claimed structural limitations are inherent in Ohtani, more particularly proving that a conventional formation of an amorphous semiconductor layer in the semiconductor structure of Ohtani includes a driving thin film transistor comprising semiconductor channels, wherein each of the semiconductor channels comprises at least one of the heterogeneous straight lines. The Examiner illustrates that the semiconductor channels do not comprise at least one of the heterogeneous straight lines; the heterogeneous straight lines are formed/located at the boundaries of the semiconductor channels.

Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. § 102(b) rejection of claims 10-13. Since none of the other prior art of record discloses or suggests all the features of the claimed invention, Applicants respectfully submit that independent claim 10, and all the claims that depend therefrom, claims 11-13, are allowable.

Claims 14-15

Claims 14 and 15 have been cancelled.

Rejections Under 35 U.S.C. § 103

In order to render a claim obvious, the combination of cited references must teach each and every element of the claimed invention and must provide teaching, motivation, or suggestion to combine. Nat'l Steel Car, Ltd. v. Canadian Pac. Rwy., 357 F.3d 1319, 1337 (Fed. Cir. 2004) (citing Ecolchem, Inc. v. S. Cal. Edison Co., 227 F.3d 1361, 1371 (Fed. Cir. 2000)). This motivation must be based on the knowledge in the art, not knowledge provided by the

application under examination, because such hindsight reconstruction is forbidden. In re Fine, 837 F.2d 1071, 1075 (Fed. Cir. 1988).

Ohtani (U.S. Patent No. 6,303,963) in view of Komiya, et. al. (U.S. Patent No. 6,456,013)

Claims 1-4, 6, 8, and 9 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Ohtani in view of U. S. Patent No. 6,456,013 issued to Komiya, *et al.*

("Komiya"). Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1, as presently amended, recites:

A flat panel display having a matrix type array of sub-pixels...wherein the driving thin film transistor comprises semiconductor channels which are derived from a semiconductor layer, and heterogeneous straight lines are separated from each other on the semiconductor layer, wherein at least one of the semiconductor channels comprise at least one of the heterogeneous straight lines, and wherein an imaginary line connecting the semiconductor channels of one column is not parallel to the heterogeneous straight lines.

Ohtani fails to teach each and every claim feature of independent claim 1, more particularly, Ohtani fails to teach at least one of the semiconductor channels comprise at least one of the heterogeneous straight lines. Rather, Ohtani teaches forming a semiconductor by crystallizing the semiconductor film using a catalytic element and then removing the catalytic element, thereby resulting in extremely small fluctuations in electrical characteristics such as threshold voltage (See col. 2, line 12 to col. 3, line 20). Thus, although Ohtani teaches formation of a semiconductor circuit, such teachings do not include or relate to the formation of heterogeneous straight lines, and more particularly to the formation of at least one of the semiconductor channels comprising at least one of the heterogeneous straight lines, as recited in amended independent claim 1.

As discussed above with respect to Ohtani, Applicants respectfully disagree that FIGS. 2D, 6B-6E, and 7A-7D illustrate the existence of heterogeneous straight lines. Figures can only anticipate claims if they clearly show the structure which is claimed (See MPEP §2125). The

figure must show all the claimed structural features and how they are put together (See MPEP §2121.04). The figures cited by the Examiner clearly do not illustrate the heterogeneous straight lines and the semiconductor channels comprising at least one of the heterogeneous straight lines. Additionally as discussed above, Applicants respectfully disagree with the Examiner's presentation that heterogeneous straight lines would be inherent from the conventional formation of channels from the amorphous semiconductor layer, wherein at least one of the semiconductor channels comprises at least one of the heterogeneous straight lines, as cited in amended independent claim 1. Rather, as taught by the Examiner, "the heterogeneous straight lines are defined at the boundary of the regions of the crystallized and regions of less crystallized" (See Office Action, on page 6, and particularly Figure 2 from Attachment provided by Examiner). Legal foundation for and explanation of inherency is described above. Applicants respectfully submit that the Examiner has failed to meet such a burden of illustrating the claimed structural limitations are inherent in Ohtani, more particularly proving that a conventional formation of an amorphous semiconductor layer in the semiconductor structure of Ohtani includes a driving thin film transistor comprising semiconductor channels, wherein at least one of the semiconductor channels comprises at least one of the heterogeneous straight lines. The Examiner illustrates the semiconductor channels do not comprise at least one of the heterogeneous straight lines; the heterogeneous straight lines are formed/located at the boundaries of the semiconductor channels.

Further, for purposes of discussion, even assuming that the heterogeneous straight lines of amended independent claim 1 may correspond to a line connecting several channel portions crystallized by a low energy periphery portion of laser light disclosed in Komiya, Komiya fails to teach or suggest any relationship between the respective channel portions crystallized by the low energy peripheral portion of laser light. Komiya only discloses an angular relationship between the gate signal line and the channel portions crystallized by the low energy periphery

portion of laser light in each TFT. Thus, Komiya is much different than claims 1-4, 6, and 8-9 of the present application, which discloses a relationship between the heterogeneous straight lines and channels in a plurality of TFTs.

Further, Komiya fails to cure the deficiencies of Ohtani for teaching or rendering obvious the claimed structural limitations for at least one of the semiconductor channels comprise at least one of the heterogeneous straight lines. Therefore, for at least the foregoing reasons, neither Ohtani nor Komiya, either alone or in combination, teaches or suggests all of the claimed features of independent claim 1. Claims 2-4, 6, 8, and 9 depend from independent claim 1, and are patentable for at least the reasons discussed above.

Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. § 103(a) rejection of claims 1-4, 6, 8, and 9. Since the none of the other prior art of record, whether taken alone or in any combination, discloses or suggests all the features of the claimed invention, Applicants respectfully submit that independent claim 1 and all the claims that depend therefrom, claims 2-4, 6, 8, and 9, are allowable.

Allowable Subject Matter

Applicants appreciate the indication that claims 5 and 7 contain allowable subject matter, acknowledging that none of the cited prior art of record, either alone or in combination, disclose or render obvious the flat panel display comprising the imaginary line connecting the semiconductor channels of one column is a zig-zag line, wherein the zig-zag line has a non-uniform zig-zag pattern, or wherein the zig-zag line has a three-step zig-zag pattern.

CONCLUSIONS

Applicants believe that a full and complete response has been made to the pending Office Action and respectfully submits that all of the stated objections and grounds for rejection have been overcome or rendered moot. Accordingly, Applicants respectfully submit that all pending claims are allowable and that the application is in condition for allowance.

Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact the Applicants' undersigned representative at the number below to expedite prosecution.

Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,

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Date: January 30, 2006

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